

10/634,174

PATENT

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

Applicant:	Leonard Forbes	Examiner:	Joannie A. Garcia
Serial No.:	10/634,174	Group Art Unit:	2823
Filed:	August 05, 2003	Docket:	1303.102US1
Title:	STRAINED Si/SiGe/SOI ISLANDS AND PROCESSES OF MAKING SAME		

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**INFORMATION DISCLOSURE STATEMENT**

MS RCE  
Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

In compliance with the duty imposed by 37 C.F.R. § 1.56, and in accordance with 37 C.F.R. §§ 1.97 *et. seq.*, the enclosed materials are brought to the attention of the Examiner for consideration in connection with the above-identified patent application. Applicant respectfully requests that this Information Disclosure Statement be entered and the documents listed on the attached Form 1449 be considered by the Examiner and made of record. Pursuant to the provisions of MPEP 609, Applicant requests that a copy of the 1449 form, initialed as being considered by the Examiner, be returned to the Applicant with the next official communication.

Pursuant to 37 C.F.R. §1.97(b), it is believed that no fee or statement is required with the Information Disclosure Statement. However, the Commissioner is hereby authorized to charge the required fees to Deposit Account No. 19-0743 in order to have this Information Disclosure Statement considered.

INFORMATION DISCLOSURE STATEMENT

Serial No :10/634,174

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Pursuant to 37 C.F.R. 1.98(a)(2), Applicant believes that copies of cited U.S. Patents and Published Applications are no longer required to be provided to the Office. Notification of this change was provided in the United States Patent and Trademark Office OG Notices dated October 12, 2004. Thus, Applicant has not included copies of any US Patents or Published Applications cited with this submission. Should the Office require copies to be provided, Applicant respectfully requests that notice of such requirement be directed to Applicant's below-signed representative. Applicant acknowledges the requirement to submit copies of foreign patent documents and non-patent literature in accordance with 37 C.F.R. 1.98(a)(2).

The Examiner is invited to contact the Applicant's Representative at the below-listed telephone number if there are any questions regarding this communication.

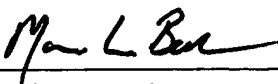
Respectfully submitted,

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By his Representatives,

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Date 7-19-06

By   
Marvin L. Beekman  
Reg. No. 38,377

CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Mail Stop RCE, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on this 19 day of July 2006.

  
Name

  
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Substitute for form 1449A/PTO

**INFORMATION DISCLOSURE  
STATEMENT BY APPLICANT**

(Use as many sheets as necessary)

Complete if Known

<b>Application Number</b>	10/634,174
<b>Filing Date</b>	August 5, 2003
<b>First Named Inventor</b>	Forbes, Leonard
<b>Group Art Unit</b>	2823
<b>Examiner Name</b>	Garcia, Joannie

Attorney Docket No: 1303.102US1

**US PATENT DOCUMENTS**

Examiner Initial *	USP Document Number	Publication Date	Name of Patentee or Applicant of cited Document	Filing Date If Appropriate
	US-20020185686A1	12/12/2002	Christiansen, S. H., et al.	04/03/2002
	US-20050285139A1	12/29/2005	Forbes, L.	08/24/2005
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	US-6,448,157	09/10/2002	Okonogi, K.	01/31/2000
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	US-7,084,429	08/01/2006	Forbes, L.	08/31/2004

**FOREIGN PATENT DOCUMENTS**

Examiner Initials*	Foreign Document No	Publication Date	Name of Patentee or Applicant of cited Document	T <sup>2</sup>
	JP-04-304653	10/28/1992	ARIMOTO, Y., et al.	English Abstract only

**OTHER DOCUMENTS -- NON PATENT LITERATURE DOCUMENTS**

Examiner Initials*	Cite No <sup>1</sup>	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T <sup>2</sup>
		Non-Final Office Action dated February 10, 2006, <u>U.S. Application Serial No. 10/979,994</u> , filed November 3, 2004, 20 pgs.	
		ANG, KAH W., "Enhanced performance in 50 nm N-MOSFETs with silicon-carbon source/drain regions", <u>IEEE International Electron Devices Meeting, 2004. IEDM Technical Digest., (Dec., 2004)</u> , 1069-1071	
		FORBES, K Y., "Non-Volatile Memory Device with Tensile Strained Silicon Layer", <u>U.S. Application No. 11/260,339</u> (client ref no 05-0753 - Leffert file), 26 pgs	
		GHANI, T., "A 90nm High Volume Manufacturing Logic Technology Featuring Novel 45nm Gate Length Strained Silicon CMOS Transistors", <u>Technical Digest IEEE International Electron Devices Meeting, (Dec., 2003)</u> , 978-980	

**EXAMINER****DATE CONSIDERED**

Substitute Disclosure Statement Form (PTO-1449)

\* EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 809. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. <sup>1</sup> Applicant's unique citation designation number (optional) <sup>2</sup> Applicant is to place a check mark here if English language Translation is attached

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(Use as many sheets as necessary)

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<b>Group Art Unit</b>	2823
<b>Examiner Name</b>	Garcia, Joannie

Sheet 2 of 2

Attorney Docket No: 1303.102US1

**OTHER DOCUMENTS -- NON PATENT LITERATURE DOCUMENTS**

Examiner Initials*	Cite No <sup>1</sup>	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T <sup>2</sup>
		GOTO, K. , "Technology Booster using Strain-Enhancing Laminated SiN (SELS) for 65nm Node Hp MPUs", IEDM Technical Digest. IEEE International Electron Devices Meeting, (Dec., 2004),209-212	
		KOMODA, T. , "Mobility Improvement for 45nm Node by Combination of Optimized Stress Control and Channel Orientation Design", IEEE International Electron Devices Meeting, 2004. IEDM Technical Digest., (Dec., 2004),217-220	
		MAIKAP, S. , "Package-strain-enhanced device and circuit performance", IEEE International Electron Devices Meeting, 2004. IEDM Technical Digest., (Dec., 2004),233-236	
		PIDIN, S. , "A Novel Strain Enhanced CMOS Architecture Using Selectively Deposited High Tensile and High Compressive Silicon Nitride Films", IEEE International Electron Devices Meeting, 2004. IEDM Technical Digest., (Dec., 2004),213-216	

**EXAMINER**

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